Amendments

In accordance with 37 CFR §1.121, please amend the above-identified application as set forth below.

Amendments to the Claims:

1. – 7. (Cancelled)

8. (Previously Presented) An On Screen Display processor for reinserting Vertical Blanking Interval data in a digital video signal comprising:

an On Screen Display controller;

a Vertical Blanking Interval waveform builder module configured to create a Video Blanking Interval Data bitmap;

an On Screen Display memory, said On Screen Display memory being configured to retain Vertical Blanking Interval position data, Vertical Blanking Interval size data and a Vertical Blanking Interval gray scale palette;

said On Screen Display controller being configured to receive the Vertical Blanking Interval data bitmap from said Vertical Blanking Interval waveform builder module and insert the Vertical Blanking Interval data bitmap into a digital video signal in operative communication with said On Screen Display controller, according to the position, size and gray scale data stored in said On Screen Display region memory; wherein an even field of said Vertical Blanking Interval data bitmap is inserted separately from an odd field of said Vertical Blanking Interval data bitmap.

9. (Original) The processor of claim 8 wherein said Video Blanking Interval Data gray scale palette remains stored in said On Screen Display memory between uses.

10. (Original) The processor of claim 8 wherein the Vertical Blanking Interval Data position data remains stored in said On Screen Display memory between uses.

11. (Original) The processor of claim 8 wherein the Vertical Blanking Interval Data size data remains stored in said On Screen Display memory between uses.

12. (Original) The processor of claim 8 wherein said On Screen Display Controller is configured to insert the Vertical Blanking Interval waveform bitmap by summing said waveform bitmap with the digital video signal.

13. (Original) The processor of claim 8 wherein the video bitstream into which the On Screen Display processor inserts the Vertical Blanking Data is configured according to MPEG protocols.

14. (Previously Presented) The processor of claim 8 wherein said video blanking interval grayscale palette is regenerated for each use.

15. (Previously Presented) The processor of claim 8 wherein said video blanking interval position data is regenerated for each use.

16. (Previously Presented) The processor of claim 8 wherein said video blanking interval size data is regenerated for each use.

17. (Previously Presented) The processor of claim 8 further comprising an input buffer in operative communication with said Vertical Blanking Interval waveform builder.

18. (Previously Presented) The processor of claim 8 further comprising an output buffer in operative communication with said Vertical Blanking Interval waveform builder.

19. (Previously Presented) The processor of claim 8 further comprising separate input buffers for even and odd fields, each of said input buffers being in operative communication with said Vertical Blanking Interval waveform builder.

20. (Previously Presented) The processor of claim 8 further comprising an integrated receiver and decoder in which said On Screen Display processor is operatively deployed.

21. (Previously Presented) The processor of claim 8 wherein said Vertical Blanking Interval waveform builder is embodied in a separate microprocessor adapted for operative communication with a processor processing media content data streams.

22. (Previously Presented) The processor of claim 8 wherein said On Screen Display controller is configured to add ancillary wave forms.

23. (Previously Presented) The processor of claim 22 wherein said On Screen Display controller is configured to add clock run in preambles.

24. (Previously Presented) The processor of claim 8 further comprising at least one additional memory region, each additional memory region being configured to retain said Vertical Blanking Interval position data, said vertical blanking interval size data, and said Vertical Blanking Interval grayscale palette.

25. (Previously Presented) The processor of claim 24 wherein further comprising at least one first memory region for even fields and at least one second memory region for odd fields.

26. (Previously Presented) The processor of claim 8 wherein said grayscale palette allocates eight bytes per pixel.

27. (Previously Presented) The processor of claim 8 further comprising a digital video serializer in operative communication with a digital video output, said digital video output receiving the output of said On Screen Display controller.

28. (Previously Presented) The processor of claim 8 wherein Vertical Blanking Interval data is displayed according to a screen space size defined at a single Vertical Blanking Interval data region.

29. (Previously Presented) The processor of claim 8 wherein Vertical Blanking Interval data is displayed according to a first Vertical Blanking Interval data size region for an even field and a second Vertical Blanking Interval data size region for an odd field.

30. (Previously Presented) The processor of claim 29 wherein each separate Vertical Blanking Interval data region has a separate grayscale palette.

31. (Previously Presented) On Screen Display processor for reinserting Vertical Blanking Interval data in a digital video signal comprising:

an On Screen Display controller;

a Vertical Blanking Interval waveform builder module configured to create a Video Blanking Interval Data bitmap;

an On Screen Display memory, said On Screen Display memory being configured to retain Vertical Blanking Interval position data, Vertical Blanking Interval size data and a Vertical Blanking Interval gray scale palette;

said On Screen Display controller being configured to receive the Vertical Blanking Interval waveform bitmap from said Vertical Blanking Interval waveform builder module and insert the Vertical Blanking Interval waveform bitmap into a digital video signal in operative communication with said On Screen Display controller, according to the position, size and gray scale data stored in said On Screen Display region memory wherein said Vertical Blanking Interval bitmap is further configured to skip every other line on an even field and skip alternate lines on an odd field.

32. (Previously Presented) An On Screen Display processor for reinserting Vertical Blanking Interval data in a digital video signal comprising:

an On Screen Display controller;

a Vertical Blanking Interval waveform builder module configured to create a Video Blanking Interval Data bitmap;

an On Screen Display memory, said On Screen Display memory being configured to retain Vertical Blanking Interval position data, Vertical Blanking Interval size data and a Vertical Blanking Interval gray scale palette;

said On Screen Display controller being configured to receive the Vertical Blanking Interval waveform bitmap from said Vertical Blanking Interval waveform builder module and insert the Vertical Blanking Interval waveform bitmap into a digital video signal in operative communication with said On Screen Display controller, according to the position, size and gray scale data stored in said On Screen Display region memory wherein said Vertical Blanking Interval waveform builder writes a bitmap to an even field memory region during the same clock cycle as an odd field memory region is read from memory.

33 – 34. (Cancelled)

35. (Previously Presented) The method of claim 8, wherein the On Screen Display memory comprises a bitmap data region and the Vertical Blanking Interval luma waveform bitmap is temporarily stored in the bitmap data region.

36. (Previously Presented) The processor of claim 8, wherein the On Screen Display memory is further configured to temporarily store the Vertical Blanking Interval Data bitmap.